Versametrics

Versatile Measurement Systems

How to Design Chips for Dart 1

The Basic Approach

The pins numbered 1-to-64 are available device pins, which would typically be grouped into pairs to make devices. For example, pins 1 & 2 might be designed to form a simple 2-terminal resistor, while pins 3 & 4 could be the contacts of a 3-terminal transistor that is gated by one of the gate pins. The gate pins are all connected and thus if a 3-terminal device is being tested then the gate must be shared by all devices on a chip (e.g., substrate gate).

Dart 1 Channels

The Dart 1 contains 2 voltage-source channels, known as the Drain and Gate channels. These Drain and Gate channels apply their voltages relative to a third reference channel (known as the Source channel). When testing transistors, we recommend using the correspondingly named channel for each device terminal. Non-transistor devices can use these channels as desired. Note that much of the documentation will discuss options assuming transistor devices under test, but feel free to adapt the information to the devices you intend to measure.

The Dart 1 socket contains 68 pins, of which 3 are hard-wired to the Gate channel, and 1 is wired to ground, as shown in the socket pinout in Figure 1. The remaining 64 pins can be programmatically routed to either the Drain or Source channels. Therefore, the Versametrics software can "select" a device by routing the Drain and Source channels to the device pins. The Gate is not electronically routable, so it is typically shared by all devices on the chip requiring a second voltage source.

Dart 1 Chip Interface

The Dart 1 has a socket to receive a chip carrier, also known as a chip package. One chip package ships with the Dart 1, and more can be purchased from Versametrics as needed. While Dart 2 aims to remove the need for wire bonding, Dart 1 requires that samples (chips) be wire-bonded into a chip package, which can then be inserted into the Dart 1 socket.

Table 1. Quick reference table of Dart 1's voltage channel capabilities.

Channel	Drain	Source	Gate
Voltage?	Yes	Grounded	Yes
Location?	Routable	Routable	Fixed

Note, chip packages can be reused many times. The diagram in Figure 1 shows a drawing of a chip package with a chip inserted, along with the pinout showing how the pins will be used by the Dart 1.

Note that the package has one pin in the center of one of the sides (pin 17) that is shaped differently than the others. This can be used to keep track of the orientation of your chip and the package. There is a corresponding triangle/arrow mark on the Dart 1 socket (that receives the package) that also

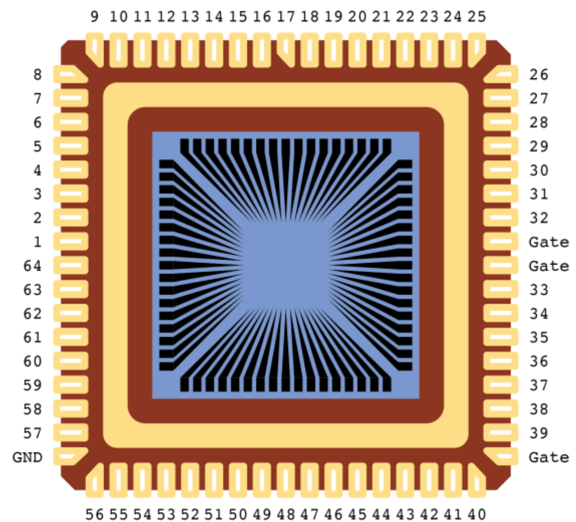


Figure 1. Dart 1 socket pinout. The ground (GND) pin is fixed in the lower left. The Gate pins are electrically connected and therefore entirely equivalent. Three Gate pins are strategically located on the right side to provide multiple options during chip layout. Pins labeled 1-64 can be either Source or Drain (software defined during testing).

marks where pin 17 is on the Dart 1. Since the gate pins on the Dart 1 are fixed, it is important that orientation be tracked such that the gate pads on samples to be tested end up connected to the fixed gate pins on the Dart 1.

Using the Gate Channel

While designing and fabricating a chip (see examples on following pages for further recommendations), plan to ensure that any connections that will use the gate terminal of the Dart 1 socket are routed near where the gate pins are located on the package (see the socket pinout indicated in Figure 1). Here are some common approaches:

1. **Substrate Gate:** Plan for the chip to be secured into the package in a manner that creates both a mechanical and electrical connection, such as silver epoxy. If the back of the chip has a dielectric layer (as is the case with thermal SiO2 on a silicon chip), this layer may need to be etched or scratched with a diamond scribe before mounting the chip into the package. Before the chip is secured (or after if space permits), a wire bond can be placed to connect one of the three gate pins on the package to the large gold pad that composes the bottom of the package where the chip sits.

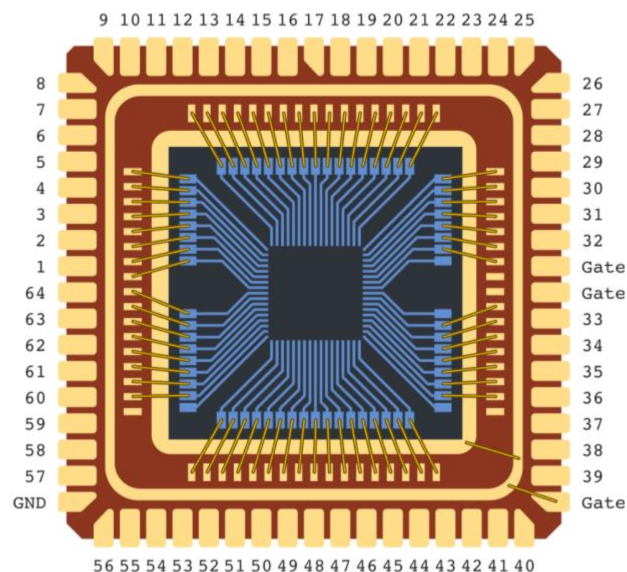
2. **Back Gate:** If a back gate has been fabricated such that it can be accessed from the top of the chip, simply fabricate an electrical connection between this gate and a wire-bondable contact pad near one of the gate pins. This will typically involve leaving or etching a hole in the gate oxide. It is also possible to treat a substrate gate in this way if a hole is similarly etched (or scratched) in the gate oxide prior to a metal deposition step.

3. **Top Gate:** Top gates, by nature of being a top layer, tend to be easily designed with a connection running to a wire-bondable pad near one of the gate pins on the package.

4. **Solution Gate:** For an on-chip solution gate electrode, such as an exposed platinum pad or a similar chlorinated silver pad, the wire bonding considerations mirror those of the top gate structure. For an off-chip solution gate (such as a Ag/AgCl electrode in a permeable glass membrane), the gate pins on the package can be left without wire bonds and an external jumper wire can be run from the gate pin on the Dart 1 IO terminal block to the external electrode.

5. **Ion-gel Gate:** Ion-gel gating can be accomplished by fabricating an exposed conductive pad that is electrically connected to a wire-bondable pad near one of the gate pins on the package. After this gate pad and the devices have been created, an ion-gel can be deposited such that it makes contact with both the devices and the gate pad. The wire-

a) Substrate Gating



b) Other Gating

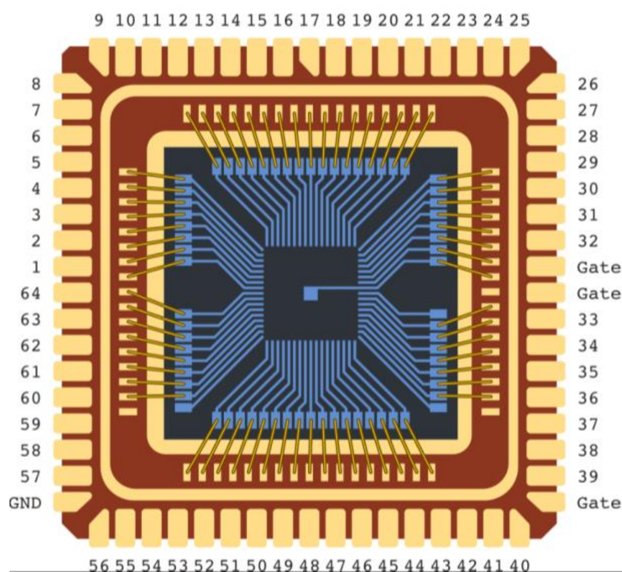


Figure 2. Diagrams of sample chips wire-bonded into packages, showing typical bond configurations for a) substrate gating, and b) other gating such as solution, top, ion-gel, or back gating that can be accessed from the top of the sample.

bondable pad connected to the gate pad can then simply be wire bonded to one of the gate pins on the package.

Example Use Cases

The following pages provide example use cases and process flows for the Dart 1 system.

#1: Nanoscale Semiconductors

Nanoscale semiconductor devices – such as research-grade field-effect transistors (FETs) made of mechanically exfoliated 2D materials or carbon nanotubes – often have nanometer-scale patterned metal contacts with very small contact pads for micromanipulators. The most common device design involves the use of a global substrate gate (i.e., global back gate), which is readily adaptable to the Dart 1 platform. Local back- or top-gate designs can also work but do require all device gates to be routed to the same gate electrode (see Figure 1 pinout diagram). Adapting FET devices to Dart 1 primarily requires an extra photolithography step during device fabrication. This lithography step defines large wire-bonding pads around the edge of a chip and several options for photomask design layouts are provided on the Versametrics website here: versametrics.com/resources/. Versametrics also offers shadow masks for direct evaporation of metal to form the large wire-bonding pads when a simplified process flow without an extra photolithography step is desired.

Fabrication Steps (Substrate Gate)

1. Prepare a clean silicon wafer with doped Si and a surface oxide layer (e.g., SiO2).
2. Use photolithography and lift-off (or direct evaporation through a Versametrics shadow mask) to define large metal pads and leads to the chip's central device area.
3. Use electron beam lithography and lift-off to define a pattern of "alignment marks" in the chip's central device area.
4. Exfoliate or transfer 2D material or nanotubes into the chip's device area.
5. Use alignment marks to locate transferred semiconductor materials precisely in CAD, by taking microscope images that contain alignment marks and material of interest.

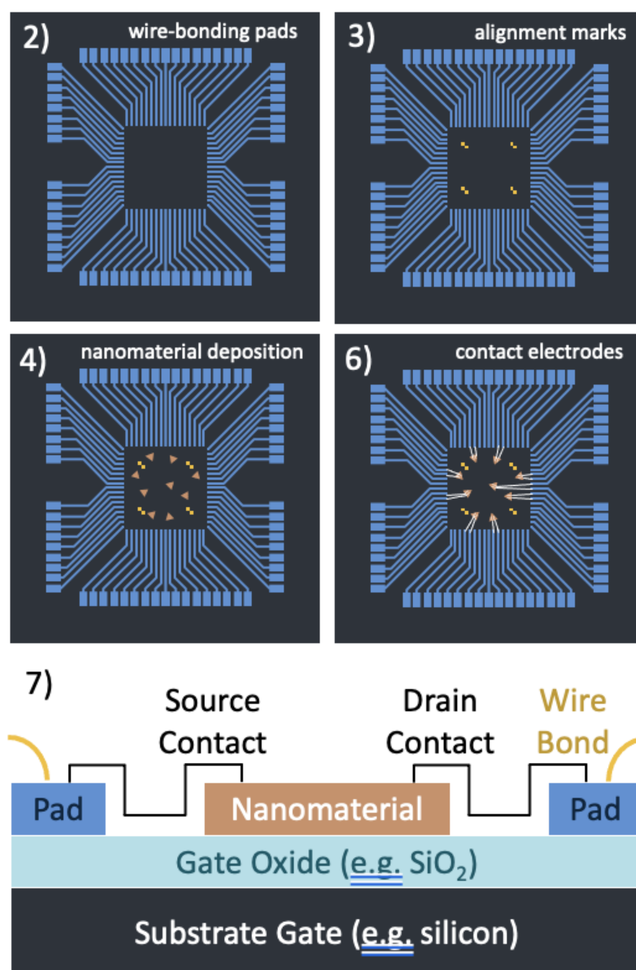


Figure 2. Diagrams of select steps for substrate-gated FETs with the corresponding step number indicated top left.

6. Use electron beam lithography and lift off to define metal contacts that connect out to large pads, completing the devices.
7. Wire-bond the peripheral large metal pads to a chip package.
8. Insert the chip package into a Dart 1 measurement platform.
9. Run automated experiments on the fabricated devices using the Versametrics software application.

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Dart 1 Documentation

#2: Printed Semiconductors

Printed semiconductor devices – such as printed carbon nanotube thin-film transistors (TFTs) – can often be fabricated rapidly in fewer steps than traditional devices. Adapting these devices to Dart 1 only requires that a suitable pattern is used to create the wire-bonding pads around the edge of a chip, which can be achieved either through printing, photolithography, or shadow mask evaporation. Several options for design layouts are provided on the Versametrics website here: versametrics.com/resources/. Versametrics also offers shadow masks for direct evaporation of metal to form the large wire-bonding pads.

Fabrication Steps (Substrate Gate)

1. Prepare a clean silicon wafer, ideally a doped wafer with a thermal oxide to act as the gate dielectric.
2. Use photolithography and lift-off to define large metal pads that lead to groups of device contacts, or accomplish the same task more simply with direct evaporation through a shadow mask provided by Versametrics.
3. Print semiconductor device channels (Fig. 3). This can either be done:
    a) Directly onto metal contacts that are already established and connected to the wire-bonding pads, OR
    b) Onto certain regions of the substrate followed by printing the contact (source/drain) electrodes connecting the semiconductor channel to the wire-bonding pads.
4. Wire bond the peripheral large metal pads to a chip package.

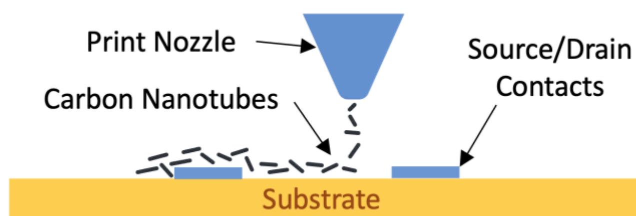
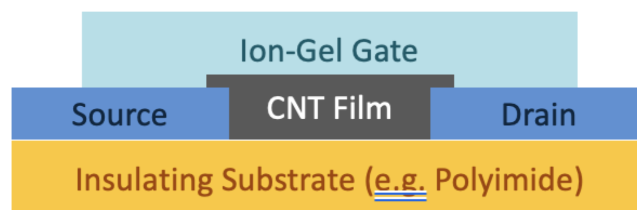


Figure 3. Printing Semiconductor Transistors. Illustration of carbon nanotubes being printed by an aerosol jet printer nozzle onto contacts on a substrate.



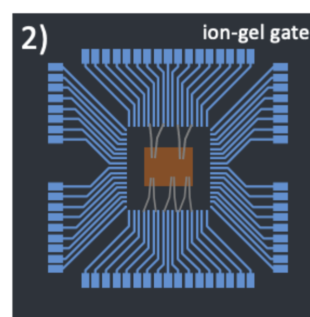


Figure 4. Ion-Gel Gate Device Structure. Schematic diagram showing a cross-sectional view of the basic structure of an ion-gel gated transistor and a schematic view of the chip with the ion-gel gate indicated.

5. Insert the chip package into a Dart 1 measurement platform.
6. Run automated experiments on the devices using the Versametrics software application.

Fabrication Steps (Ion Gel Gate)

1. Same first three steps as outlined for the Substrate Gate devices in the instructions to the left.
2. After establishing the semiconducting channel and the source/drain electrodes, print ion gel (or other ionic dielectric) that overlaps the printed channels and the large center gate electrode (see Figure 4).
3. Insert the chip package into a Dart 1 measurement platform.
4. Run automated experiments on the devices using the Versametrics software application.

Wire Bonding Guide

To make electrical connection to devices on a semiconductor chip, there are two main options: a temporary spring-probe connection or a permanent wire-bonded connection. Wire bonding offers some advantages over the use of traditional micromanipulator-based probes, such as: a highly reliable and permanent connection, a slim and unobtrusive form-factor once installed, and avoiding the need to frequently move probes manually around a delicate chip to make and remake connections. While Dart 2 aims to remove the need for wire bonding while still providing a reliable electrical interface, Dart 1 still requires wire bonding, and provides that option for users who are comfortable with wire bonding. Wire bonders are used in the semiconductor packaging industry, and they are also often available in university research facilities (such as the West Bond model 747677E shown in the figure below).

A wire bonder is made up of at least a few critical components: 1) a heated stage, 2) a hollow needle which feeds metal wire to form the actual bonds, and 3) a microscope and other controls to aid the operator in accurate placement of the wire bonds. Some wire bonders are automatic, but most basic models are manually controlled.

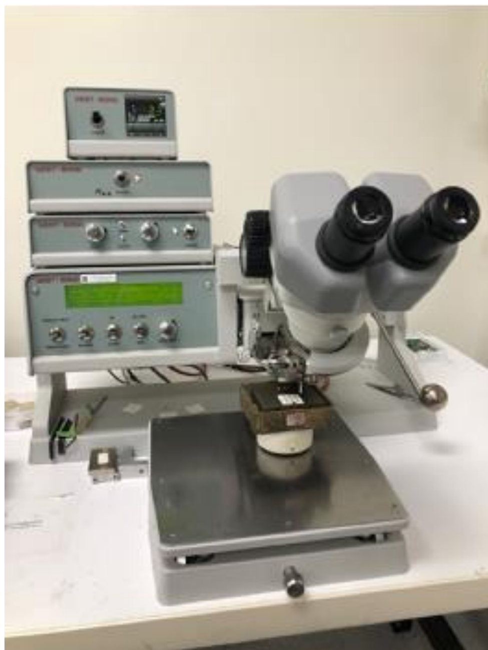


Figure 5. West Bond model 747677E.

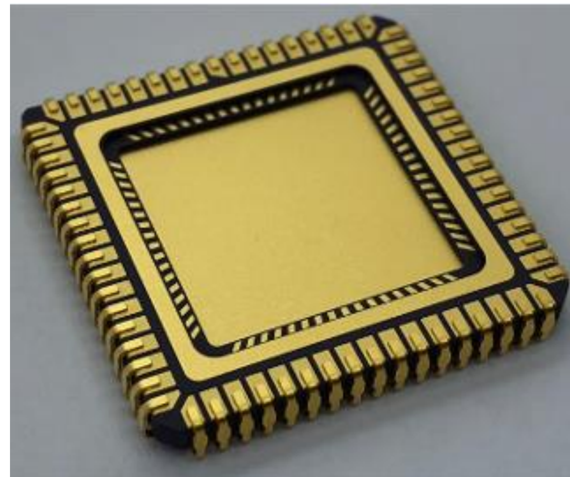


Figure 6. PLCC 68-pin chip carrier package.

To wire bond a sample to a chip package, a suitable chip carrier package must first be obtained. The Dart 1 is compatible with PLCC 68-pin chip carrier packages, such as the one shown below (one of these packages ships with the Dart 1, and more can be purchased from the Versametrics Store).

Several types of samples could be secured in such a package, with common examples including devices fabricated on substrates such as silicon chips, polyimide, quartz, glass, and ceramics. An example of a typical sample, in this case a silicon

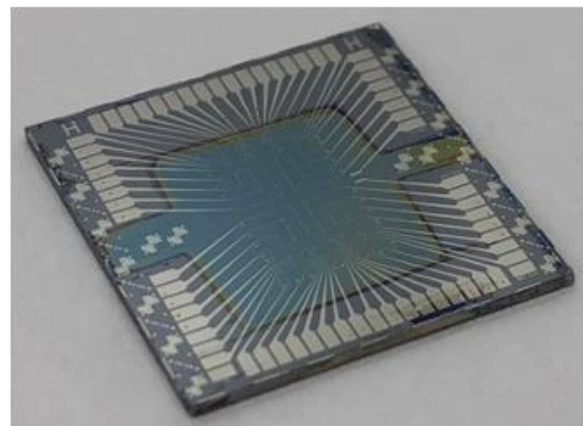


Figure 7. Silicon chip with metal interconnects and 68 large pads (~1mm) around the edges ready for wire bonding.

chip with devices fabricated on its surface using freely available Versametrics layout files, is shown below.

Most commonly, wire bonding will consist of forming electrical connections between the metal pads near the periphery of the sample chip and the corresponding pads on the package. The gold thread wire bonds can be seen spanning between the pads on the chip and the pads on the package in the figure below.

If it is necessary to form an electrical contact with the back of the chip (e.g. for a substrate gate), there are several steps which must be taken before wire bonding the rest of the chip. In the center of each chip carrier is a recessed cavity that receives the chip, and to make a connection with the back of the chip it is critical for the chip to be well-connected with the gold coating at the bottom of this cavity. This can be done in a variety of ways, such as conductive paint, conductive epoxy, or conductive tape, but simply placing the chip into the cavity dry is often not enough to make good contact. However, regardless of the chosen method of bonding the chip into the cavity, the gold coating at the bottom of the cavity also needs to be wire bonded to one of the gate pins shown in the Dart 1 socket pinout. Note that this can be done well beforehand, while the chip carrier is empty as shown in the figure below. Our recommended way of doing this is the following 2-step method:

1. Make an intermediate connection from the gold at the bottom of the chip cavity up to the gold rail that runs around the perimeter of the chip carrier (as shown in the figure below).

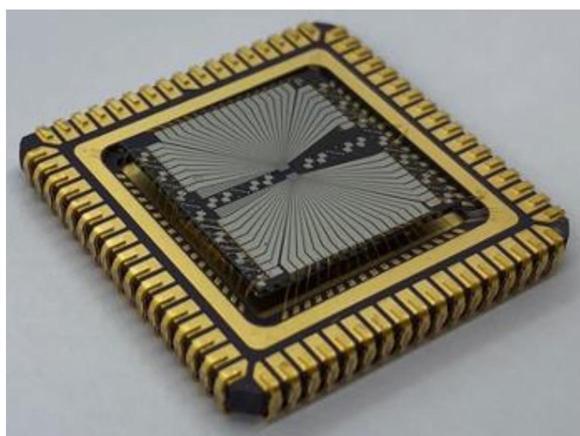


Figure 8. Example chip that has been wire bonded to a 68-pin PLCC chip carrier package.

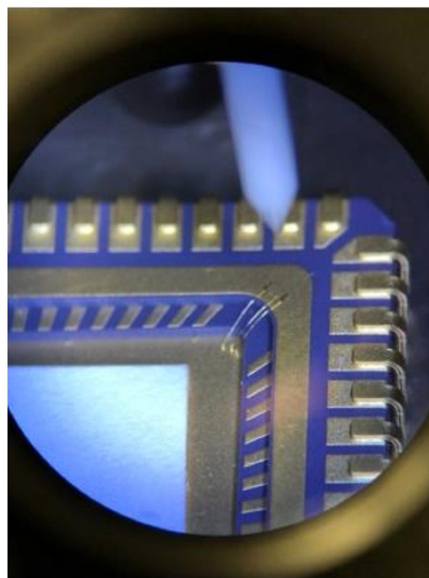


Figure 9. Wire bonds formed between the bottom of the sample cavity and the annular gold rail/bus of the chip carrier package. Three bonds were formed for redundancy, and the bonds were created before the sample was mounted in the chip carrier package.

2. Connect the intermediate rail to any of the 3 gate pins of the Dart 1 pinout, such as the conveniently located corner gate pin (as shown in the figure below).

For a substrate gate, we conventionally recommend using the gate pin in the corner, simply because it is out of the way of all the other pins. The centrally located gate pins are often used for a global top gate/solution gate/ion-gel gate and can be left unconnected when using a substrate gate.

If an electrical connection to the substrate is not required, such as when using top gating, solution gating, or other forms of gating not reliant on the substrate, the flow is somewhat simpler. The sample must still be secured in the chip package, but no electrical connections need to be made or ensured at that stage of packaging. In this case, the sample can be secured into the cavity of the chip carrier package by any suitable mechanical means, such as a small dab of glue, epoxy, or double-sided tape on the bottom of the sample. The main requirement is that any materials used be able to withstand wire bonding temperatures (typically at or below 150 C).

Once the chip has been secured in the package (with or without ensuring an electrical connection, as appropriate), it is time to perform the wire bonding process connecting the pads of the sample to the pads on the chip carrier package. The first step is to mount the chip carrier package containing the sample onto the stage of the wire bonder, then heat the stage to the desired temperature (125 C for the wire bonder in this example). Note that the stage will typically need to be heated 25 to 50 C hotter than the machine recommends for a sample that is not in a package, as the heat flow dynamics cause the chip surface to be cooler when it is separated from the stage by the package than when it is mounted on the stage directly.

With the chip package mounted on the wire bonder stage and preheated, it is time for a wire bond to be formed between each pad on the chip carrier package and the corresponding pad on the sample/chip. We recommend starting each wire bond on the chip and terminating the bond on the chip carrier package. Consult the user manual for your wire bonder for more specific instructions on the steps involved. Note that the chip carrier package has a thick gold layer that is ideal for promoting great adhesion of a wire bond, but it is often not practicable to utilize such a thick or ideal layer on a sample/chip. While a gold layer with a thickness of several hundred nanometers is frequently recommended for pads that will receive a wire bond, we have seen good results wire bonding to silicon chips with pads made from 30 nm thick platinum or 30 nm thick palladium, both with an underlying adhesion layer of 1 nm titanium.

When making wire bonds, take care that the bonds do not cross, touch another bond, or contact anything that you do not intend for them to make electrical contact with. One common pitfall is the edge of the sample. If the sample has a conductive substrate (e.g. doped silicon) and the wire bonds touch the edge of the chip, the bonds can be shorted with or through the substrate. This can occur even if the sample has an insulating coating on the top surface (e.g. SiO_2), as frequently this coating has been damaged at the edge of the sample when the sample was diced or cleaved from a larger source material. This shorting through the substrate is more likely when the sample is elevated in the package and the wire bonds are pulled tight, and it can be avoided by taking care to form the wire bonds in a shape that ensures they touch only the source and destination wire bonding pads.

Especially when dealing with a manual wire bonder, it may seem daunting to manually form roughly 68 bonds to package a single chip. While it may take a sample or two in the beginning for a user to become proficient, our experience is that once a user has been trained it takes on the order of 5 minutes to bond all 68 connections. This burden tends to be reasonable, but Versametrics intends to remove both the need of a wire bonding machine and the need to perform wire bonding through the Dart 2, which is currently under development. Once released, this approach will make it much easier to measure the same sample at various stages of fabrication/processing.

Example Wire Bonder Settings

Here are wire bonder settings that we frequently use with an ultrasonic wire bonder. For more details consult your wire bonder instruction manual.

Precise settings values will depend on the wire-bonder in use. For the West Bond wire bonder featured in this guide, all settings were left at the default value except for the work holder temperature, which was increased by 50 C. As a reference, the settings used for the featured wire bonder are shown in the table below.

Table 2. Recommended settings for wire bonding with a West Bond model 747677E.

Setting	Value
Bonds per wire	2
Lift before torch	350
Ultrasonic power Bond 1	275
Ultrasonic power Bond 2	285
Ultrasonic time Bond 1	30
Ultrasonic time Bond 2	30
Force Bond 1	Low
Force Bond 2	High
Loop Height	50
Wire Tail	100

Dual Force	On
Ball Fault	On
Beep upon contact	On
Bond counter	On
Bond counter limit	25000
U/S power during feed	500
NEFO Power	6.3
NEFO Time	2.5
Work Holder temperature	150
Wire	0.001" Au

Sample Fabrication Steps for Wire Bonding

Your sample fabrication process is likely quite unique. In case your existing process needs any adaptations to become compatible with wire bonding, we provide an example fabrication process for reference in the following detailed steps:

1. Start with a silicon wafer with 90 nm thermal oxide
2. Spin LOR 2A at 500 RPM for 5 s then 3000 RPM for 30 s, with acceleration 1000 RPM/s
3. Bake on hot plate at 180 C for 5 min
4. Spin S1813 resist at 500 RPM for 5 s then 3000 RPM for 30 s, with acceleration 1000 RPM/s
5. Bake at 115 C for 60 s
6. Expose for 10 s at 365 nm with "Versametrics Mask 2" mask
7. Develop for 100 s in MF-319
8. Evaporate 1 nm Ti, 30 nm Pt
9. Lift-off Pt/Ti/S1813/LOR in NMP at 80 C for 1 hour
10. Rinse in an acetone bath for 1 min
11. Rinse in IPA for 30 s
12. Blow dry in nitrogen
13. Perform further fabrication steps specific to this sample…
14. Wire bond into package at 200 C

Using the Packaged Chip with Dart 1

Once the chip has been properly packaged and wire bonded as described in the previous sections, the package can be inserted into the socket on the Dart 1, with proper attention being paid to orientation, as discussed above. At that point, the Dart 1 can be plugged in to a computer, the Versametrics software can be launched, and experiments can be queued up and run on the devices to be tested.