How to Design Chips for Dart 1

The Basic Approach

The pins numbered 1-to-64 are available device pins, which would typically be grouped into pairs to make devices. For example, pins 1 & 2 might be designed to form a simple 2-terminal resistor, while pins 3 & 4 could be the contacts of a 3-terminal transistor that is gated by one of the gate pins. The gate pins are often shared by many devices on a chip.

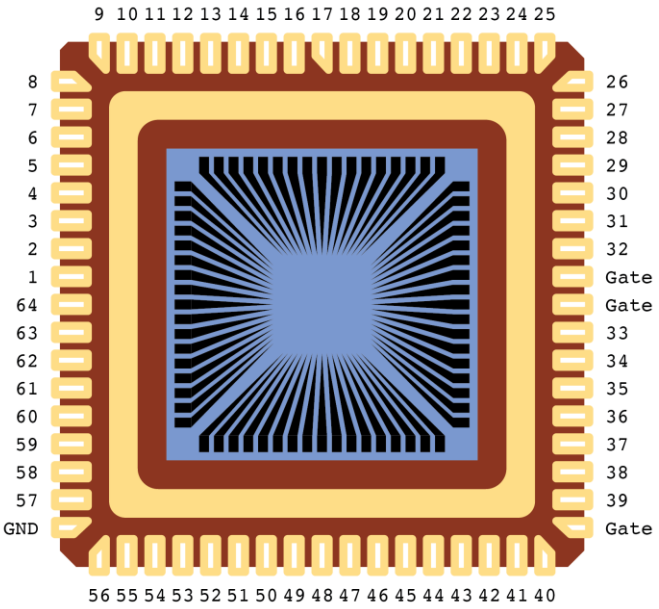
Dart 1 Channels

The Dart 1 contains 2 voltage-source channels, known as the “Drain” and “Gate” channels. These Drain and Gate channels apply their voltages relative to a third reference channel (known as the "Source” channel). When testing transistors, we recommend using the correspondingly named channel for each device terminal.

The Dart 1 socket contains 68 pins, of which 3 are hard-wired to the Gate channel, and 1 is wired to ground. The remaining 64 pins can be programmatically routed to either the Drain or Source channels. Therefore, the system is able to “select” a device by routing the Drain and Source channels to the device pins. The Gate is not electronically routable, so it is typically shared by all devices on the chip.

Channel:	Drain	Source	Gate
Voltage?	Yes	Reference	Yes
Location?	Routable	Routable	Fixed

Dart 1 Socket Pinout



Gates: the 3 “Gate” pins on Dart 1 are electrically connected and entirely equivalent. They are strategically located in 3 places for flexibility in chip layout and ease-of-access.

Dart 1 Chip Interface

The Dart 1 has a socket to receive a chip carrier, also known as a chip package. One chip package ships with the Dart 1, and more can be purchased from Versametrics as needed. While Dart 2 aims to remove the need for wire bonding, Dart 1 requires that sample chips be wire-bonded into a chip package, which can then be inserted into the Dart 1 socket. The diagram above shows a drawing of a chip package with a chip inserted, along with the pinout showing how the pins will be used by the Dart 1.

Wire Bonding Guide

Overview

Wire bonding has many advantages over the use of tools like micromanipulators for making contact to electrical devices that need to be tested, such as highly reliable contact over long periods of time, ability to withstand vibrations, increased ability to allow access to the chip by other instruments during electrical testing, and lack of a necessity to frequently move probes manually around a delicate chip to make and remake connections. While Dart 2 aims to remove the need for wire bonding while still providing a reliable electrical interface for long term experiments, using wire bonding on chips to be tested with Dart 1 still allows access to these advantages.

Managing the Gate

While designing and fabricating a chip (see examples on following pages for further recommendations), plan ahead to ensure that gate connections are routed near where the gate pins are located on the package (see Socket Pinout on page 1). Here are some common approaches:

1. *Substrate Gate:* Plan for the chip to be secured into the package in a manner that creates both a mechanical and electrical connection, such as silver epoxy. If the back of the chip has a dielectric layer (as is the case with thermal SiO_2 on a silicon chip), this layer may need to be etched or scratched with a diamond scribe before mounting the chip into the package. Before the chip is secured (or after if space permits), a wire bond can be placed to connect one of the three gate pins on the package to the large gold pad that composes the bottom of the package where the chip sits.
2. *Back Gate:* If a back gate has been fabricated such that it can be accessed from the top of the chip, simply fabricate an electrical connection between this gate and a wire-bondable contact pad near one of the gate pins. This will typically involve leaving or etching a hole in the gate oxide. It is also possible to treat a substrate gate in this way if a hole is similarly etched (or scratched) in the gate oxide prior to a metal deposition step.
3. *Top Gate:* Top gates, by nature of being a top layer, tend to be easily designed with a connection running to a wire-bondable pad near one of the gate pins on the package.
4. *Solution Gate:* For an on-chip solution gate electrode, such as an exposed platinum pad or a similar chlorinated silver pad, the wire bonding considerations mirror those of the top gate structure. For an off-chip solution gate (such as a Ag/AgCl electrode in a permeable glass membrane), the gate pins on the package can be left without wire bonds and an external jumper wire can be run from the gate pin on the Dart 1 IO terminal block to the external electrode.
5. *Ion-gel Gate:* Ion-gel gating can be accomplished by fabricating an exposed conductive pad that is electrically connected to a wire-bondable pad near one of the gate pins on the package. After this gate pad and the devices have been created, an ion-gel can be deposited such that it makes contact with both the devices and the gate pad. The wire-bondable pad connected to the gate pad can then simply be wire bonded to one of the gate pins on the package.

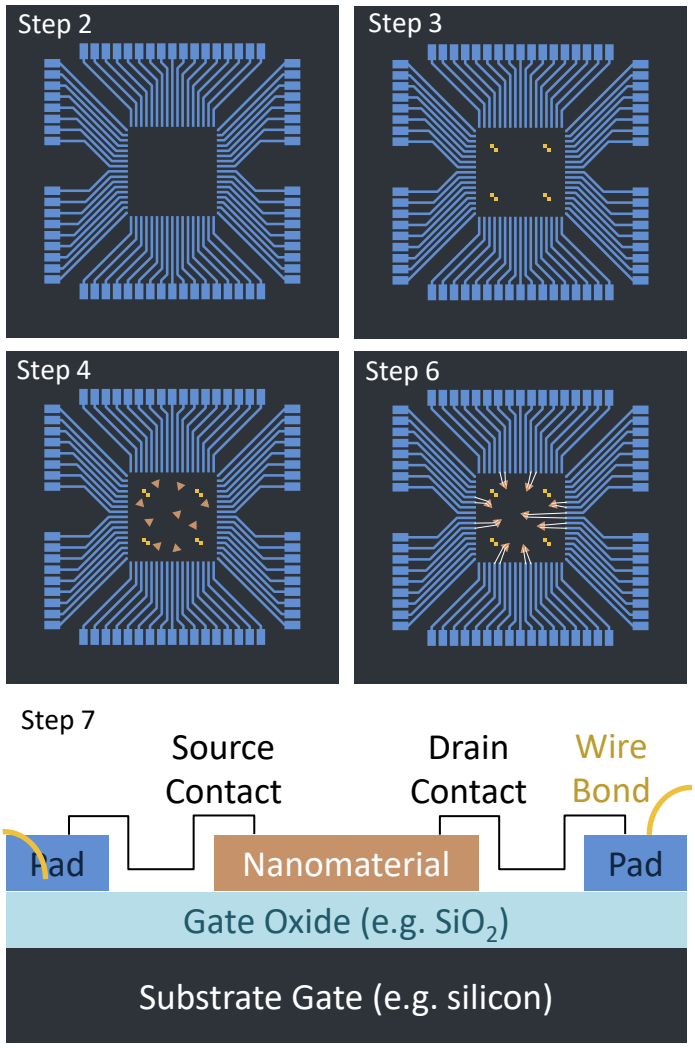
Note that wire bonding to a chip in a package on the wire bonder heating platform often requires a higher temperature on the platform than when bonding to a chip resting directly on the platform in order to achieve a similar temperature at the chip surface.

Example 1:
Nanoscale Semiconductor Devices

Nanoscale semiconductor devices – such as research-grade devices made of mechanically exfoliated 2D materials or individual carbon nanotubes – often have nanometer-scale patterned metal contacts with very small contact pads for micromanipulators. Adapting these devices to Dart 1 primarily requires an extra photolithography step before device fabrication. This lithography step defines large wire-bonding pads around the edge of a chip. Versametrics also offers shadow masks for direct evaporation when a simplified process flow without an extra photolithography step is desired.

Suggested Fabrication Steps (Back Gate)

1. Prepare a clean silicon wafer.
2. Use photolithography and lift-off (or direct evaporation through a Versametrics shadow mask) to define large metal pads and leads to the chip's central device area.
3. Use electron beam lithography and lift-off to define a pattern of "alignment marks" in the chip's central device area.
4. Exfoliate or transfer 2D material or nanotubes into the chip's device area.
5. Use alignment marks to locate transferred semiconductor materials precisely in CAD, by taking microscope images that contain alignment marks and material of interest.
6. Use electron beam lithography and lift off to define metal contacts which connect out to the larger leads (defined in Step 2, refer to Socket Pinout on page 1), completing the devices.
7. Wire bond the peripheral large metal pads to a chip package (see Wire Bonding Guide on page 2).
8. Insert the chip package into a Dart 1 measurement platform.
9. Run automated experiments on the fabricated devices using the Versametrics software application.



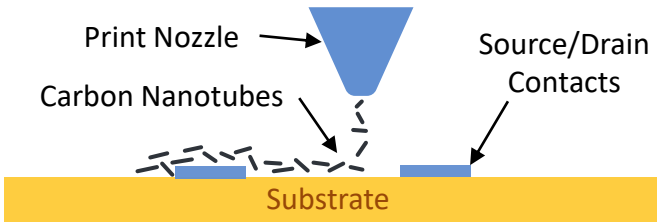
Fabrication Steps: Diagrams of select steps with the corresponding step number indicated top left.

Example 2:
Printed Semiconductor Devices

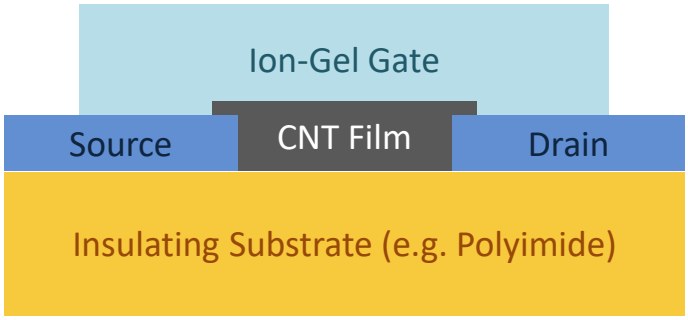
Printed semiconductor devices – such as printed carbon nanotube thin-film transistors – can often be fabricated rapidly in fewer steps than traditional devices. Adapting these devices to Dart 1 only requires that a suitable photolithography pattern is used to create the wire-bonding pads around the edge of a chip.

Suggested Fabrication Steps (Back-Gate)

1. Prepare a clean silicon wafer, ideally a doped wafer with a thermal oxide to act as the gate dielectric.
2. Use photolithography and lift-off to define large metal pads which lead to groups of device contacts, or accomplish the same task more simply with direct evaporation through a shadow mask provided by Versametrics.
3. Print semiconductor device channels directly onto metal contacts.
4. Wire bond the peripheral large metal pads to a chip package (see Wire Bonding Guide on page 2).
5. Insert the chip package into a Dart 1 measurement platform.
6. Run automated experiments on the fabricated devices using the Versametrics software application.



Printing Semiconductor Transistors: Illustration of carbon nanotubes being printed by an aerosol jet printer nozzle onto contacts on a substrate.



Ion-Gel Gate Device Structure: Schematic diagram showing a cross sectional view of the basic structure of an ion-gel gated transistor.

Suggested Fabrication Steps (Ion-Gel Gate)

1. Prepare a clean substrate of quartz, polyimide, silicon with a thermal oxide layer, or similar dielectric material.
2. Use photolithography and lift-off to define large metal pads which lead to groups of device contacts, and a single large center gate electrode. Alternatively, accomplish the same task more simply via direct evaporation through a shadow mask provided by Versametrics.
3. Print semiconductor device channels directly onto metal contacts.
4. Print ion gel that overlaps the printed channels and the large center gate electrode.